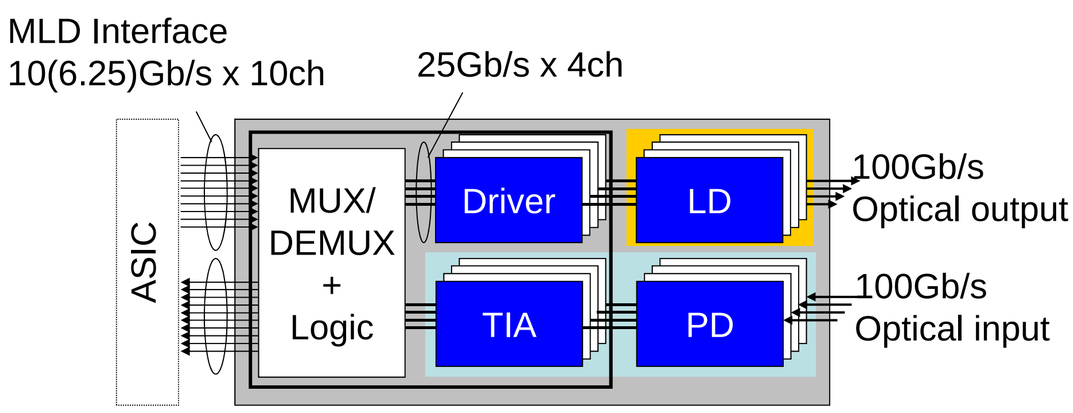
Key Device Technologies for 100Gb/s Micro-Optical Module

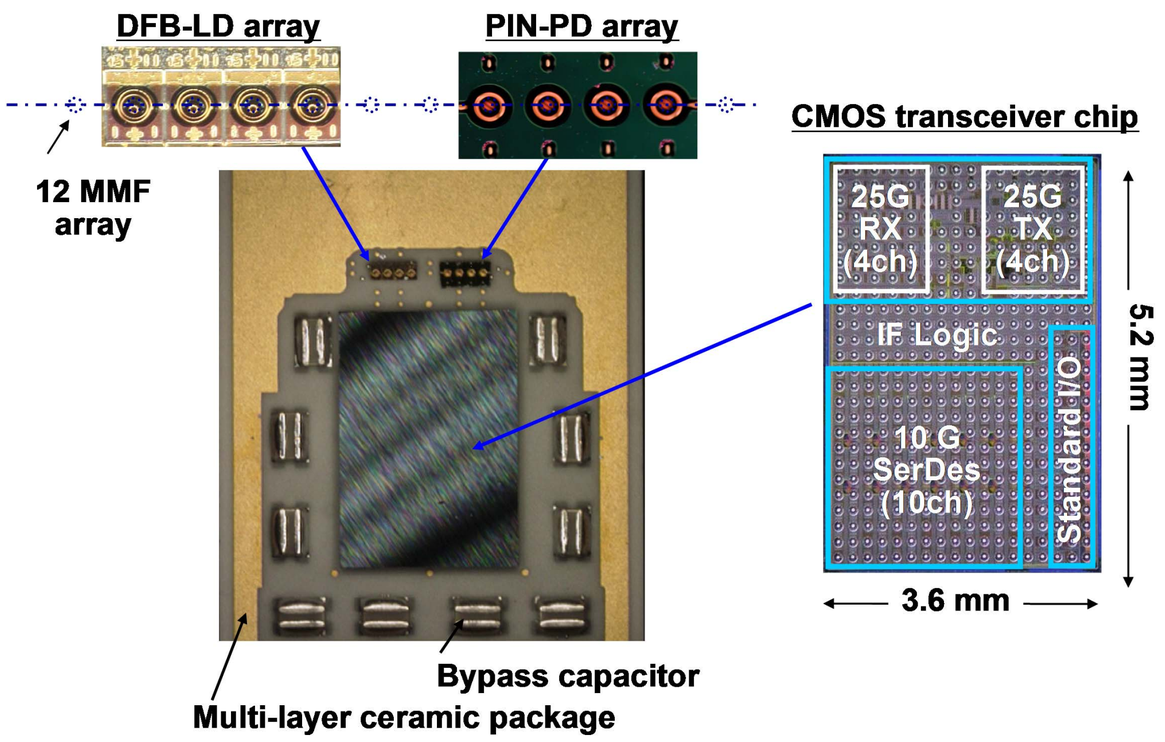
TECHNICAL CHALLENGES

- High speed Front-end CMOS Circuits, and One-chip Integration with MUX/ DEMUX and Logic Circuits
- High-speed Laser-array with Vertical Optical Access
- Hybrid integration on a common substrate



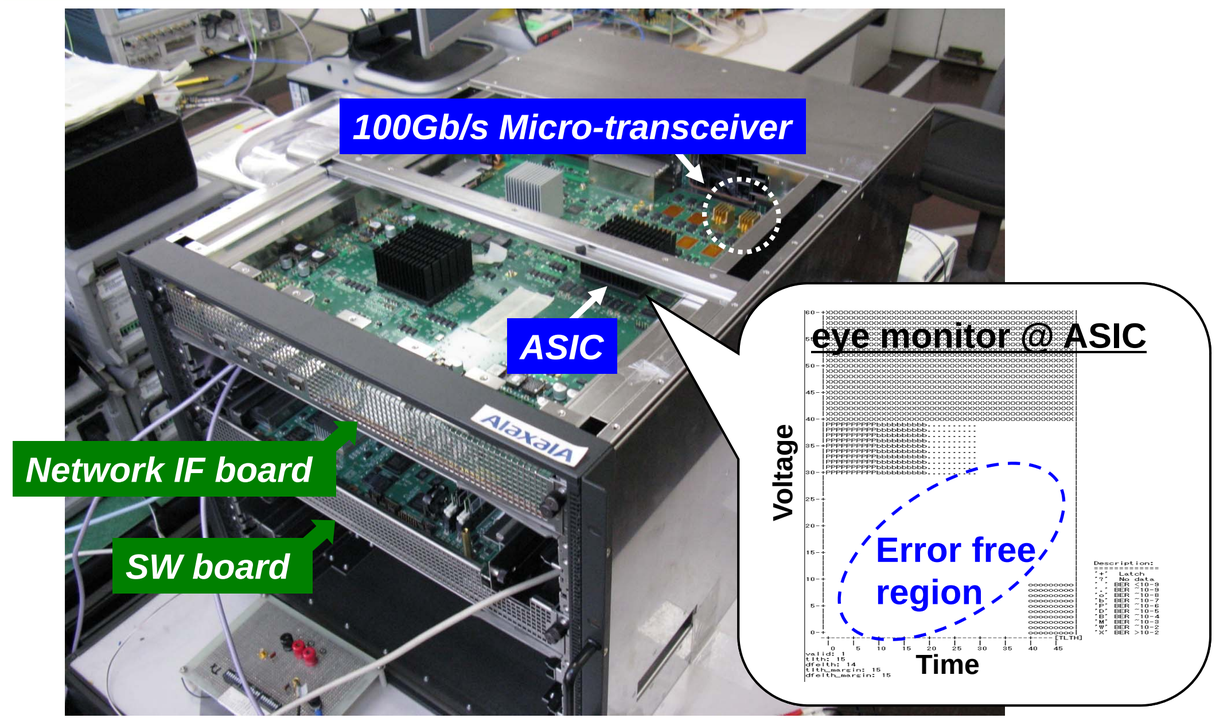
100Gb/s Micro-transceiver Structure

KEY ACCOMPLISHMENTS



Inside of the 100Gb/s Micro-transceiver

Signal Transmission



Error Free Signal Transmission in a Router

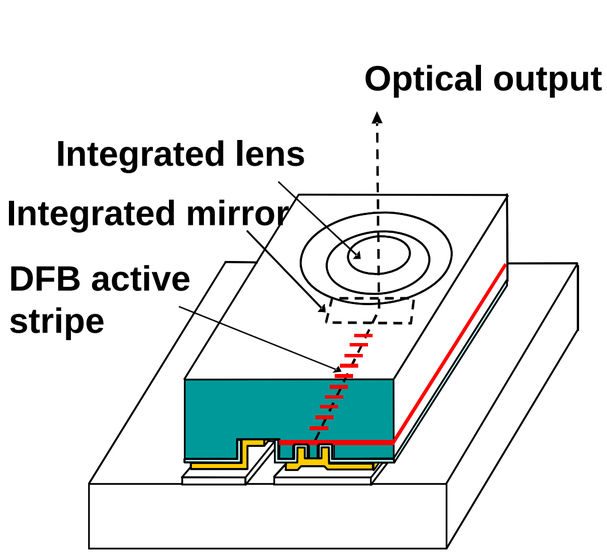
CMOS Transceiver Chip

- High speed CMOS F/E: 25Gb/s
- Low power: 20mW/Gb/s
  - One chip integration
  - Quarter rate operation for Rx circuits
  - Dynamic circuits for 10G SerDes

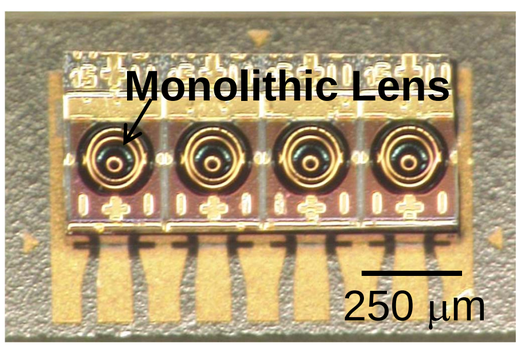
CMOS Transceiver LSI Block Diagram

Surface Emitting DFB Laser

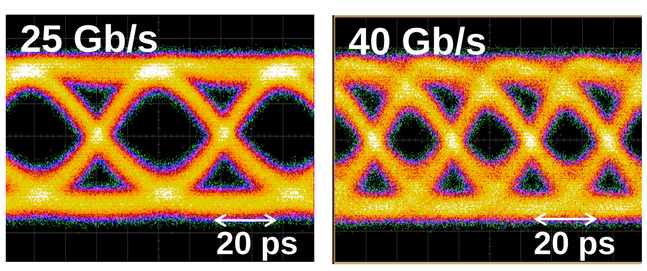
- Low threshold: 15mA at 85°C, 1.3 μm
- High speed: 4ch x 25Gb/s (25-85 °C)
- Surface emission, SMD electrodes



Laser structure



Top view (4ch array)



Waveform

AlaxalA Empowered by Innovation NEC HITACHI Inspire the Next PETRA

Next-generation High-efficiencyNetwork Device Technology Project